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Date of mailing (day/month/year) 07 June 2000 (07.06.00)	
International application No. PCT/GB99/03100	**Applicant's or agent's file reference** RL.P50896PC
International filing date (day/month/year) 17 September 1999 (17.09.99)	**Priority date** (day/month/year) 13 October 1998 (13.10.98)
Applicant KUBICZEK, Maciej et al	

1. The designated Office is hereby notified of its election made:

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9/806490

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :		(11) International Publication Number:	WO 00/22507
G06F 9/00	A2	(43) International Publication Date:	20 April 2000 (20.04.00)

(21) International Application Number: PCT/GB99/03100

(22) International Filing Date: 17 September 1999 (17.09.99)

(30) Priority Data:
9822191.4 13 October 1998 (13.10.98) GB

(71) Applicant *(for all designated States except US)*: DIGITAL COMMUNICATION TECHNOLOGIES LTD. [GB/GB]; The Kingston Business Exchange, 12–50 Kingsgate Road, Kingston, Surrey KT2 5AA (GB).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: KUBICZEK, Maciej [PL/GB]; 3 Westbrook Avenue, Hampton, Middlesex TW12 2RE (GB). TURNER, Christopher, Robert [GB/GB]; 3 Westbrook Avenue, Hampton, Middlesex TW12 2RE (GB).

(74) Agent: LIND, Robert; Marks & Clerk, 4220 Nash Court, Oxford Business Park South, Oxford OX4 2RU (GB).

(81) Designated States: GB, JP, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: MICROPROCESSOR

(57) Abstract

A microprocessor (10) incorporating a modified Harvard architecture connected to two memory banks (100) and (114). The main CPU also includes two pushdown stacks (104, 108). One of the stacks has its top two items connected directly to an arithmetic–logic unit (103). In addition hardware is provided to perform seven operations on the top three stack elements. The instruction length of the microprocessor is 8 bits and most instructions execute in a single clock cycle. A unique feature of the instruction set is that 128 of the 256 possible bytecodes are user–programmable. Some regular instructions can be "folded" with the "return from subroutine" instruction. This allows the efficient implementation of a wide variety of virtual machines, such as the Java Virtual Machine. The microprocessor also contains dedicated registers and circuits for the efficient implementation of dynamic variables (112), 32–bit immediate constants (109 and 110), interfaces to dedicated co–processors and interfaces to local area networks allowing dynamic upgrades of application software.

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MICROPROCESSOR

The present invention relates to a simplified instruction set microprocessor. More particularly, though not necessarily, the invention relates to a microprocessor which may be used to implement a version of the Java Virtual Machine.

High level language oriented computer architectures have been known for many years, but until now few of them have been successful commercially. Currently, the most popular computer architectures are either general-purpose Complex Instruction Set Computers (CISC) such as the Intel 80x86 family of microprocessors, or general-purpose Reduced Instruction Set Computers (RISC).

The success of the Java programming language, and the demands which the Java environment places on an execution platform, may change this situation. This means that language specific architectures may in the future become more popular as a Java-oriented architecture is likely to be more efficient in executing Java than a general-purpose microprocessor.

Java is a young technology and has been designed to run on a variety of computing platforms, but the benefits of using dedicated special-purpose architectures have been apparent from the outset. SUN Microsystems™, the originators of Java, have developed a microprocessor core called picoJava™. This core is targeted toward the high-end of the computer market, i.e. it is intended for use in large desktop computer type applications. picoJava™ is large, complex and power-hungry, making it unsuitable for smaller, embedded types of applications.

Certain similarities between the Java Virtual Machine and the Forth programming language have led manufacturers of Forth chips to re-brand their chips as Java chips. While some Forth chips are better at implementing Java than other general-purpose microprocessors,

differences between the Java Virtual Machine and Forth ensure that a dedicated Java microprocessor will generally outperform a Forth microprocessor.

Embedded systems often operate under stringent real-time constraints. In particular, the interrupt latency of a processor is a critical parameter. With complex microcoded instructions, interrupt latency can be on the order of several dozen or even hundreds of clock cycles.

It is an object of the present invention to provide a high-performance, virtual machine tailored microprocessor with a reduced transistor count compared to other processors, such as existing Java processors.

It is also an object of this invention to provide a high-performance microprocessor, which has the low interrupt latency necessary in many real-time embedded systems.

It is a further object of the invention to provide extremely good code density for high-level language generated programs.

It is a further object of the invention to simplify the translation process from a machine independent bytecode representation of a program, such as the Java Virtual Machine bytecodes, to the microprocessor's instruction set, so that "on the fly" application program loaders, such as the Java class loaders, can be implemented at minimal cost.

It is a further object of the invention to provide a means for the microprocessor to communicate with other microprocessors via a local area network, and to enable software upgrades to be performed remotely over the network.

It is a further object of the invention to provide the means for the microprocessor to interface directly to a dedicated slave co-processor (such as a numeric co-processor, a digital signal processor (DSP), a special purpose communication processor, etc.) so that special purpose systems can be easily implemented.

According to a first aspect of the present invention there is provided a microprocessor system comprising:

a central processing unit;

an instruction memory for storing a sequence of instructions which correspond either to a fixed and predefined operation or to a user defined operation; and

means for fetching each stored instrucion in turn and for analysing each instruction to determine whether an instruction corresponds either to a fixed and predefined operation or to a user defined operation and, in the former case, for passing the instruction to the central processing unit for execution or, in the latter case, for calling a subroutine corresponding to the instruction.

Preferably, instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code. Thus, the means for analysing each stored instruction is arranged to check for the presence of a bit in that bit position.

Preferably, the microprocessor system comprises a data memory arranged in use to store code defining said subroutines. More preferably, the system comprises means for generating an address corresponding to the location of a subroutine if an instruction corresponds to user defined operations. Where said distinguishing bit is the most significant bit of the instruction code, this means is arranged to shift the code to the left by one or more bits. Preferably, the microprocessor comprises a program counter register which is arranged to load the bit shifted instruction.

Preferably, the microprocessor system comprises a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory when execution of the subroutine is completed.

Preferably, the central processing unit, instruction memory, data memory, hardware stack, and program counter are all coupled to a common bus. More preferably, all of these components including the bus are integrated onto a single chip.

Preferably, the instruction memory is arranged to hold 8-bit wide instructions, whilst the data memory is arranged to hold 32-bit data values.

Preferably, the central processing unit contains an arithmetic logic unit and a data stack. The top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

Preferably, the top three elements of the data stack contain special-purpose circuits, which enable the efficient (single cycle) execution of seven primitive stack operations directly in hardware. The remaining data stack elements are simple shift registers.

Preferably, the microprocessor system has a means for recognising a "fast return" instruction "folded" with a regular instruction, by utilising circuitry which decodes the "fast call" bit in the 8-bit bytecode and another dedicated bit (or bits) in the 8-bit bytecode. More preferably, this other bit (or bits) is (are) the second (and subsequent) most significant bit(s) in the 8-bit bytecode.

Preferably, the microprocessor contains a dedicated register called the *Parameter Pool Pointer*, together with associated circuitry and several dedicated instructions for storing and accessing 32-bit quantities in data memory using short (8-bit or 16-bit) offsets. This mechanism allows the efficient implementation of local (dynamic) variables in block and object oriented languages.

Preferably, the microprocessor contains a dedicated register called the *Global Constant Pool Pointer*, together with associated circuitry and dedicated instructions for storing and accessing 32-bit quantities in data memory using short (8-bit or 16-bit) offsets. This mechanism allows the efficient implementation of 32-bit literal constants, which are global to all execution contexts, using only an 8-bit or 16-bit bytecode extension.

Preferably, the microprocessor contains a dedicated register called the *Local Constant Pool Pointer*, together with associated circuitry and dedicated instructions for storing and accessing 32-bit quantities in data memory using short (8-bit or 16-bit) offsets. This allows

the efficient implementation of 32-bit literal constants, which are local to a particular execution context.

Preferably, the microprocessor contains a dedicated register called the *Extension Stack Pointer*, together with dedicated circuits, which is used to spill data stack elements into data memory, and to refill the data stack from data memory.

Preferably, the microprocessor contains dedicated circuitry, to efficiently implement a subroutine call via an in-memory jump table, which is essential for an efficient implementation of dynamic method dispatch in object oriented programming languages. In a preferred embodiment of this invention this language would be the Java programming language.

Preferably, the microprocessor contains dedicated circuitry and instruction to improve the efficiency of exception handlers.

Preferably, the microprocessor contains dedicated hardware mechanisms to allow the efficient implementation of a variety of garbage-collection algorithms, which are essential in many object-oriented systems, such as Java.

Preferably, the microprocessor contains circuits for interfacing the microprocessor to a data network and to allow the microprocessor's software to be dynamically upgraded over that network.

Preferably, the microprocessor contains a means for communicating with a special-purpose co-processor, such as a DSP processor or a math processor. The co-processor can be integrated on the same silicon die as the microprocessor, or can be located off-chip.

According to a second aspect of the present invention there is provided a method of processing a set of instructions in a microprocessor system, the method comprising:

extracting instructions in sequence from an instruction memory, where said instructions correspond either to a fixed and predefined operation or to a user defined operation;

analysing each extracted instruction to determine whether the instruction corresponds either to a fixed and predefined operation or to a user defined operation;

in the former case, passing the instruction to the central processing unit for execution; and

in the latter case, calling a subroutine corresponding to the instruction.

According to a third aspect of the present invention there is provided a microprocessor system comprising a central processing unit, an 8-bit wide bytecode memory, a 32-bit data memory, and busses connecting the central processing unit with the two memories.

For a better understanding of the present invention and in order to show how the same may be carried into effect reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 illustrates schematically a microprocessor system;

Figure 2 illustrates schematically a fast subroutine call mechanism of the system of Figure 1;

Figure 3 illustrates schematically a the folding of a subroutine return operation in the system of Figure 1;

Figure 4 illustrates schematically immediate operand decode logic of the system of Figure 1; and

Figure 5 illustrates schematically a data stack of the system of Figure 1.

Figure 1 shows a block diagram of a microprocessor 10. It is seen that the microprocessor 10 has a simple architecture. The central processing unit is connected to two memories: an 8-bit wide Bytecode Memory 100 and a 32-bit wide Data Memory 114. The CPU contains a main Arithmetic Logic Unit 103 and two hardware stacks: the Return Stack 104 and the Data Stack 108. The top two elements of the Data Stack 108 are connected directly to the inputs of the ALU 103. The CPU also contains an 8-bit Instruction Register 101 for latching the currently executing instruction bytecode, and an Immediate Operand circuit 102 which connects the output of the Bytecode Memory to the CPU's Internal Data Bus 115. The CPU also contains a Program Counter register 105, which is connected to the input of the Bytecode Memory Address ALU 106 and also to the input and output ports of the Return Stack 104. In addition to the above, the CPU also contains four dedicated

address registers, namely the Global Constant Pool Pointer 109, the Local Constant Pool Pointer 110, the Extension Stack Pointer 111, and the Parameter Pool Pointer 112. The read ports of the address registers are connected to the input of the Data Memory Address ALU 113.

Figure 2 shows a block diagram of the fast subroutine call mechanism. The microprocessor instruction fetch logic includes a circuit which distinguishes a bit 150 (the most significant bit in a preferred embodiment of the invention) in the 8-bit instruction register 101 which latches a bytecode fetched from a bytecode memory 100. If the bit 150 is active, the microprocessor program counter is loaded with the output of the Address Generator circuit 151 which uses the remaining 7 bits of the bytecode to produce an address. In a preferred embodiment of the invention, the circuit 151 shifts the low 7 bits left by two bits. The program counter register load is determined by the control signal on gate 152. At the same time, the current value of the program counter 105 is stored in the on-chip return stack 104. This sequence of actions is performed in a single clock cycle, and is equivalent to a fast subroutine call to one of 128 possible locations.

Figure 3 shows the block diagram of the circuit implementing the folding of a subroutine return operation with a regular instruction. The microprocessor instruction decode logic includes a circuit which tests two bits 150, 200 in the 8-bit instruction register 101 which latches a bytecode fetched from bytecode memory, and controls a circuit 201, which reloads the program counter register from the top of the return stack. In a preferred embodiment of the invention the two bits would be the two most significant bits in the 8-bit bytecode. This action is performed in parallel with normal instruction execution, and means that any (regular) instruction of the microprocessor can be "folded" with a return from subroutine operation, effectively providing a zero-overhead operation.

The fast call/fast return features of the microprocessor allow very short instruction sequences to be encoded as 8-bit user-defined bytecodes. This feature is a key to providing good code density and also good interrupt latency, since the "macro" instructions are composed of a sequence of simple (RISC-like) machine instructions of the microprocessor, and can be interrupted without problems.

The instruction fetch logic of the microprocessor includes a circuit, shown in Figure 4, which allows a bytecode to be followed by a single 8-bit immediate value. This immediate value is read from bytecode memory 100 and latched in the immediate operand module 102. Depending on the bytecode, this 8-bit value can be combined with one of the address registers 109, 110, 111, 112, shown in Figure 4 as reference numeral 250, to provide an address into data memory, from which a full 32-bit immediate value is fetched.

The organisation of the Data Stack is shown in Figure 5. The top three data stack entries 300 are different from the remaining stack entries 301 and are provided with special-purpose circuits, which enable them to execute seven primitive stack manipulation operations directly in hardware in one clock cycle. The top two elements of the Data Stack are connected to the inputs of the microprocessor's Arithmetic Logic Unit 103. The stack manipulation primitives have been selected to either directly correspond to some Java Virtual Machine stack manipulation instructions, and to allow the composition of the remaining Java Virtual Machine instructions from two or three primitives. The primitive operations are:

- POP Remove the top stack element
- DUP Duplicate the top stack element
- OVER Copy the second stack element over the top stack element
- SWAP Swap the top two stack elements
- LROT Rotate the top 3 stack elements left
- RROT Rotate the top 3 stack elements right
- TOVER Copy the third stack element over the top stack element

The remaining Data Stack elements 301 are implemented as a simple array of 32 by n shift registers.

Object-oriented languages, such as Java, require the efficient implementation of local (or dynamic) variables. The microprocessor here described supports the concept of a *Parameter Pool*. A parameter pool is an area of data (32-bit) memory, with individually addressable locations. The addresses of the individual locations are small positive integers.

The Parameter Pool is implemented using a dedicated pointer register called the *Parameter Pool Pointer* register. Hardware mechanisms are provided for transferring data from the data stack to the Parameter Pool, and for accessing and storing individual elements in the pool using either a short (8-bit) offset in the bytecode stream, or a 32-bit offset from the top of the data stack.

A 32-bit architecture requires 32-bit literal constant operands to be included in the instruction set. Current practice in bytecoded architectures is to embed the literal constant in the bytecode stream. This increases the code size, and makes the instruction decoding circuits more complex. The approach taken with the present microprocessor is the provision of *constant pools*, which hold the values of the literal constants. Two pools are provided for each execution context. A *Global Constant Pool* contains literal constants common to all execution contexts (the most commonly occurring constants, plus constants for the operation of the virtual machine). A *Local Constant Pool* contains literal constants specific to a particular execution context. The constant pools are implemented using two dedicated pointer registers: *the Global Constant Pool Pointer* register and the *Local Constant Pool Pointer* register. Hardware mechanisms are provided to enable the initialisation of the constant pools and the efficient retrieval of any constant from the pools using an 8-bit offset in the bytecode stream, or a 32-bit offset from the top of data stack.

The on-chip data stack is used for expression evaluation. In a preferred embodiment of the invention the depth is equal to 8, which is adequate for most situations. The (relatively) shallow depth of the data stack makes context switching faster, since in the case in question only at most 8 elements need to be spilled into memory. In some cases, the number of elements on the data stack may exceed 8, causing stack overflow. To deal with this situation a dedicated register, called the *Extension Stack Pointer* is provided, together with dedicated circuits for loading/storing the bottom element of the data stack in data memory, according to the address stored in the Extension Stack Pointer.

Object oriented languages use dynamic method dispatch very extensively. The present microprocessor implements dynamic method dispatch using subroutine calls via a jump table. This operation is performed using a built-in instruction of the microprocessor.

Many modern programming languages, such as Java, include facilities for defining exception handlers. The present microprocessor has instructions and dedicated circuits to improve the efficiency of the implementation of exception handlers.

Modern high-level programming languages, such as Java, use sophisticated memory management techniques based on garbage collection. The present microprocessor contains circuits, which allow the efficient implementation of a variety of garbage collection algorithms, for different application areas.

Since the "semantic gap" between the microprocessor here described and typical stack-based virtual machine architectures is small, it is possible to implement very simple dynamic loaders, which allow machine-independent application code (such as software upgrades) for the microprocessor to be downloaded over a local data network. In a preferred embodiment of the invention, the machine-independent code would be the Java class file format. For this reason, the microprocessor contains a unit for connecting the processor to a local area network.

Many modern embedded systems consist of a control module and a data-processing module. The control module is usually implemented by a general-purpose microprocessor, while the data processing part is implemented by a dedicated hardware processor. Depending on the application area, the dedicated hardware processor can be a digital signal processing (DSP) processor, or a special-purpose math co-processor. To allow the present microprocessor to be used in such situations, special purpose instructions have been provided in the microprocessor, together with dedicated circuitry enabling the processor to directly interface to a wide variety of special-purpose co-processors.

The microprocessor described above has the following important distinguishing features:

- Low transistor count and low power dissipation for use in small embedded systems
- Unique two-level architecture involving a fast *micro machine* and a slower *macro machine*
- Modified Harvard architecture with an 8-bit wide *bytecode memory* and a 32-bit wide *data memory*.

- Bytecode (0-operand) instruction set for maximum code density.
- 32-bit internal architecture.
- A 32-bit wide hardware operand stack coupled to the ALU, with automatic fill/spill unit.
- A 32-bit wide hardware return (subroutine) stack, with automatic fill/spill unit.
- RISC-like instruction set, with most instructions executing in a single cycle.
- Zero-overhead subroutine return instruction which can be "folded" with other instructions.
- 128 user-programmable bytecodes facilitating the efficient creation of virtual machines.
- Hardware support for the efficient execution of high-level languages, such as Java.
- Global and local constant pools, allowing the specification of 32-bit immediate constants using short offsets in the bytecode stream.
- Parameter pool, allowing the efficient implementation of local variables.
- Hardware and instructions for dynamic method dispatch
- Hardware and instructions for the efficient implementation of software exceptions
- Hardware support for garbage collection algorithms
- Interface to a local area network for dynamic upgrading of the application software
- Hardware interface to a variety of on- and off-chip co-processors

It will be appreciated by the person of skill in the art that various modifications may be made to the above described embodiments without departing from the scope of the present invention.

CLAIMS

1. A microprocessor system comprising:

a central processing unit;

an instruction memory for storing a sequence of instructions which correspond either to a fixed and predefined operation or to a user defined operation; and

means for fetching each stored instrucion in turn and for analysing each instruction to determine whether an instruction corresponds either to a fixed and predefined operation or to a user defined operation and, in the former case, for passing the instruction to the central processing unit for execution or, in the latter case, for calling a subroutine corresponding to the instruction.

2. A microprocessor system according to claim 1, wherein instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code, and the means for analysing each stored instruction is arranged to check for the presence of a bit in that bit position.

3. A microprocessor system according to claim 1 or 2, wherein the microprocessor system comprises a data memory arranged in use to store code defining said subroutines.

4. A microprocessor system according to claim 3, wherein the system comprises means for generating an address corresponding to the location of a subroutine if an instruction corresponds to a user defined operations.

5. A microprocessor system according to claim 4, wherein said distinguishing bit is the most significant bit of the instruction code, and the generating means is arranged to shift the code to the left by one or more bits.

6. A microprocessor system according to claim 5 and comprising a program counter register which is arranged to load the bit shifted instruction.

7. A microprocessor system according to any one of claims 3 to 6, wherein the instruction memory is arranged to hold 8-bit wide instructions, whilst the data memory is arranged to hold 32-bit data values.

8. A microprocessor system according to any one of the preceding claims and comprising a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory when execution of the subroutine is completed.

9. A microprocessor system according to claim 8, wherein the central processing unit, instruction memory, data memory, hardware stack, and program counter are all coupled to a common bus.

10. A microprocessor system according to claim 9, wherein the central processing unit, instruction memory, data memory, hardware stack, program counter, and common bus are integrated onto a single chip.

11. A microprocessor system according to any one of the preceding claims, wherein the central processing unit contains an arithmetic logic unit and a data stack, and the top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

12. A microprocessor system according to claim 11, wherein the top three elements of the data stack contain special-purpose circuits, which enable the execution of seven primitive stack operations directly in hardware.

13. A microprocessor system according to any one of the preceding claims and comprising means for recognising a "fast return" instruction "folded" with a regular instruction, by utilising circuitry which decodes the "fast call" bit in an 8-bit bytecode and another dedicated bit or bits in the 8-bit bytecode.

14. A microprocessor system according to claim 13, wherein said other dedicated bit is the second most significant bit in the 8-bit bytecode.

15. A microprocessor system, consisting of a central processing unit, 8-bit wide instruction memory, 32-bit wide data memory and a hardware stack connected via an internal bus to the program counter register, together with an instruction decode unit which includes a circuit for detecting the presence of a distinguished bit in the 8-bit bytecode, together with a circuit for loading the remaining bits of the bytecode shifted left by a number of bits into the microprocessor's program counter register, while at the same time storing the current value of the program counter register on the aforementioned stack.

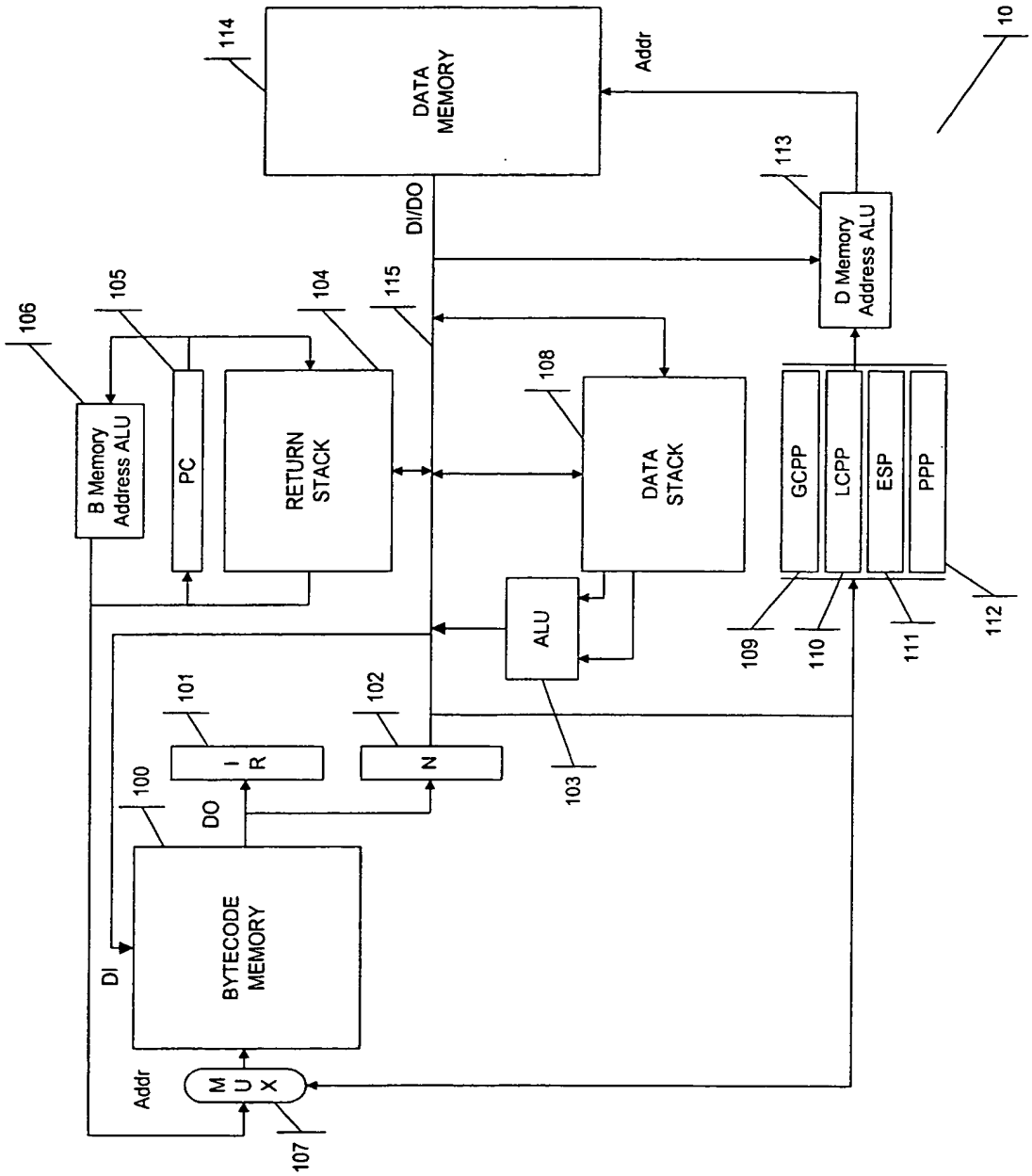
10
114
DATA MEMORY
Addr
113
D Memory Address ALU
DI/DO
115
104
105
106
108
B Memory Address ALU
PC
RETURN STACK
DATA STACK
GCPP
LCPP
ESP
PPP
ALU
109
110
111
112
101
102
I R
N
103
100
DO
BYTECODE MEMORY
DI
Addr
M U X
107

Figure 1

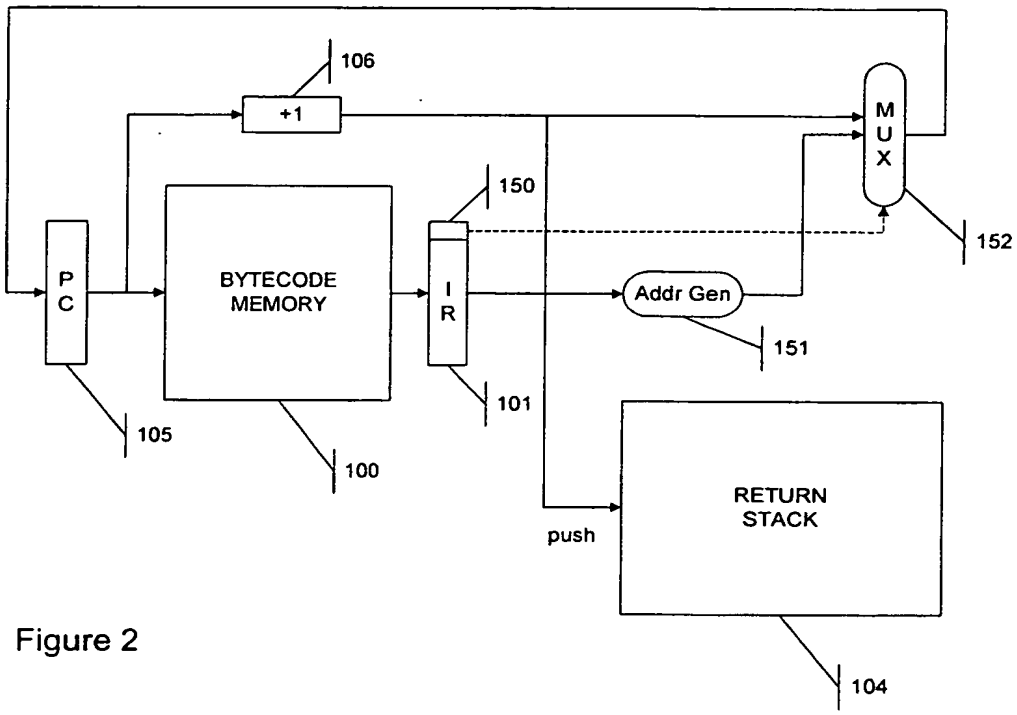
106
+1
M
U
X
150
152
P
C
BYTECODE
MEMORY
I
R
Addr Gen
151
101
105
100
RETURN
STACK
push
104

Figure 2

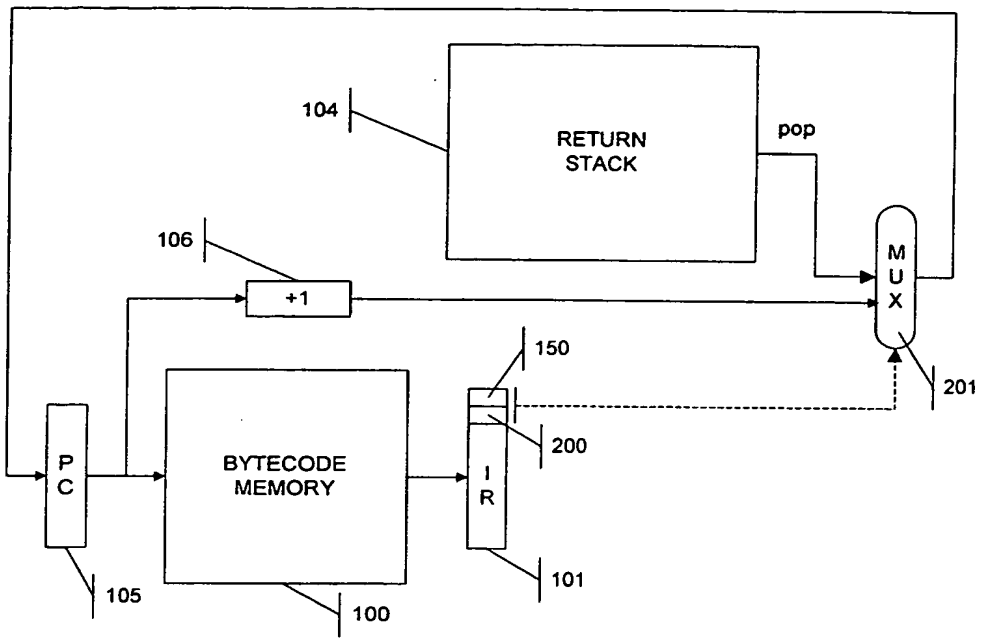
104
RETURN STACK
pop
106
+1
M U X
150
201
200
P C
BYTECODE MEMORY
I R
105
100
101

Figure 3

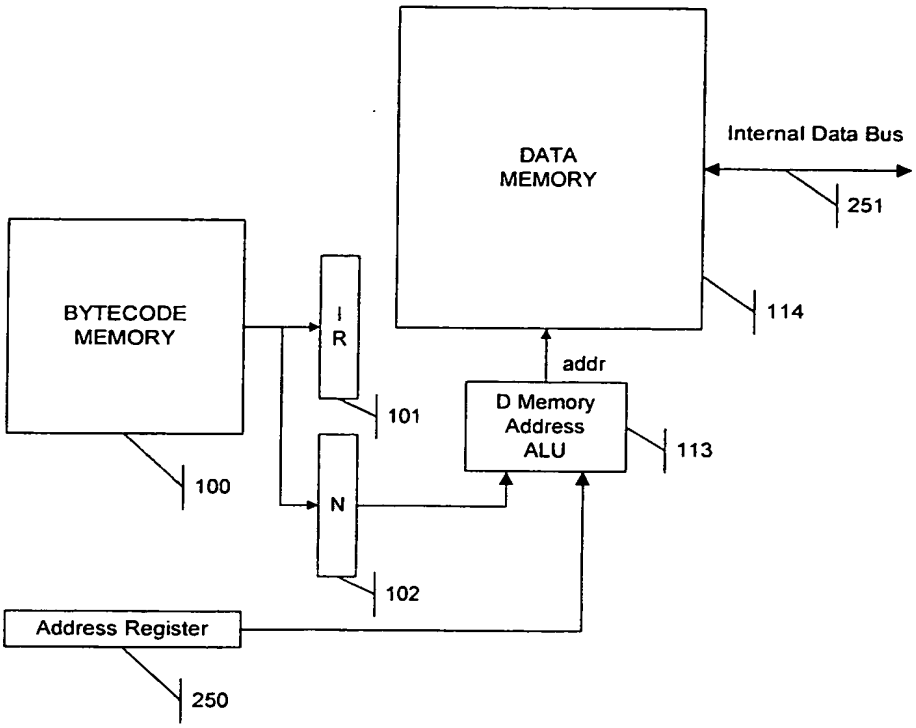
DATA
MEMORY
Internal Data Bus
251
114
BYTECODE
MEMORY
I
R
101
addr
D Memory
Address
ALU
113
100
N
102
Address Register
250

Figure 4

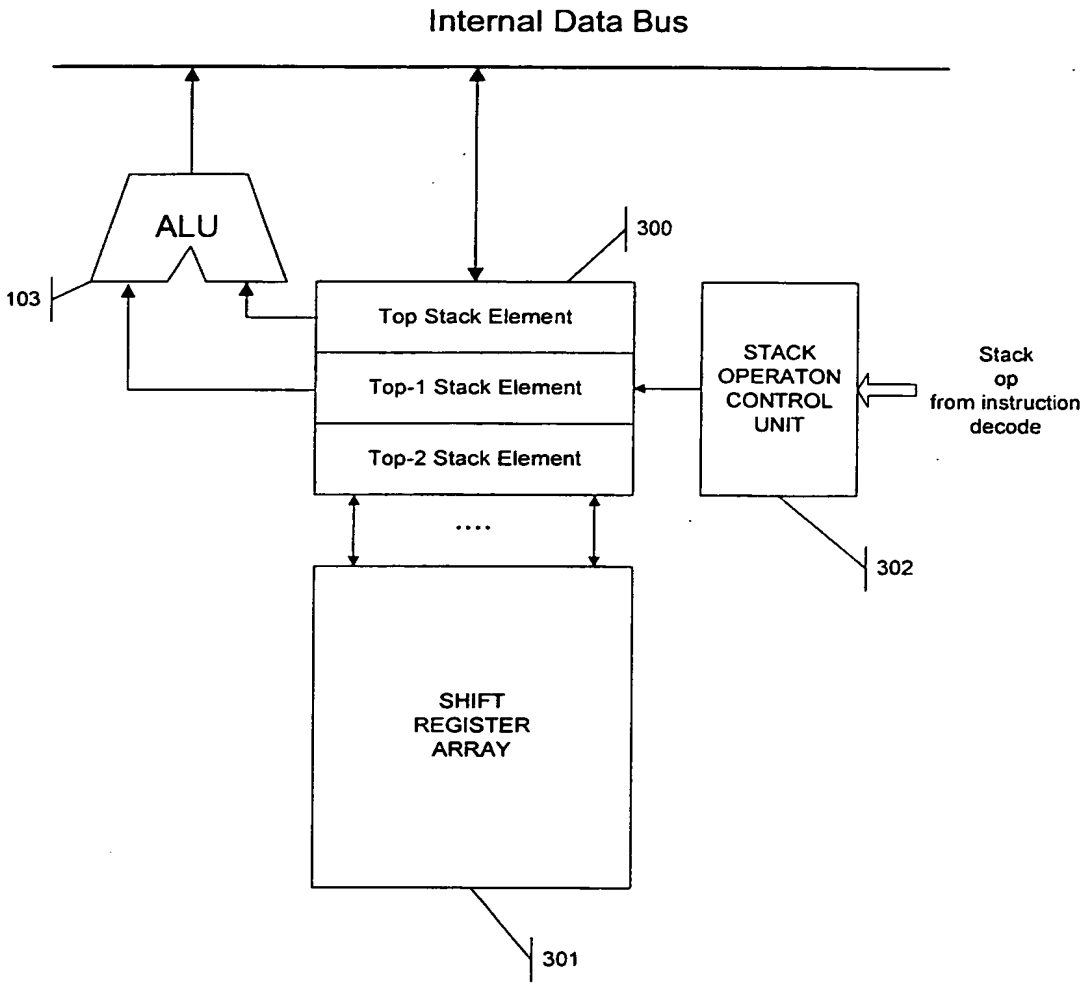
Internal Data Bus
ALU
103
300
Top Stack Element
Top-1 Stack Element
Top-2 Stack Element
....
STACK OPERATON CONTROL UNIT
Stack op from instruction decode
302
SHIFT REGISTER ARRAY
301

Figure 5

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

To:
MARKS & CLERK
Attn. Lind, Robert
4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU
UNITED KINGDOM

Date of mailing *(day/month/year)*	26/04/2000
Applicant's or agent's file reference: RL.P50896PC	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/GB 99/03100	International filing date *(day/month/year)* 17/09/1999

Applicant

DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.

1. [X] The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Fascimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

[ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

[ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

Within **19 months** from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within **20 months** from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lucia Van Pinxteren

Form PCT/ISA/220 (July 1998)

NOTES FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see Volume II of the PCT Applicant's Guide.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
RL.P50896PC		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 99/03100	17/09/1999	13/10/1998
Applicant		
DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 5 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [X] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/03100

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/318

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 479 621 A (DURANTON MARC) 26 December 1995 (1995-12-26)	1,3,4,8
A	column 2, line 43 - line 46 column 4, line 10 - line 49 column 9	15

X	EP 0 279 953 A (TEXAS INSTRUMENTS INC) 31 August 1988 (1988-08-31)	1,3,4
Y	column 3, line 25 - line 27 column 3, line 43 -column 4, line 24 column 4, line 45 - line 55 column 5, line 13 - line 37 column 6, line 7 - line 16	2
A	column 7	2,15

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2000	26.04.00

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Moraiti, M

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ROGERS: "Emulation instruction" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 25, no. 11A, page 5576-5577-5577 XP002112146 ISSN: 0018-8689	1,3,4
Y	the whole document	2,5,6
Y	US 5 752 073 A (GRAY III DONALD M ET AL) 12 May 1998 (1998-05-12) column 14, line 18 - line 24 figure 7	2,5,6
X	"REAL-TIME CISC ARCHTECTURE HW EMULATOR ON A RISC PROCESSOR" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 37, no. 3, page 605 XP000441601 ISSN: 0018-8689 the whole document	1,3,4
P,A	WO 99 31579 A (MOTOROLA INC) 24 June 1999 (1999-06-24) page 10, line 1 -page 11, line 10	1,3,4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/03100

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5479621 A	26-12-1995	FR 2678401 A	31-12-1992
		DE 69229302 D	08-07-1999
		DE 69229302 T	02-12-1999
		EP 0520579 A	30-12-1992
		JP 5189240 A	30-07-1993
EP 0279953 A	31-08-1988	DE 3750721 D	08-12-1994
		DE 3750721 T	16-03-1995
		JP 63228225 A	22-09-1988
		US 5235686 A	10-08-1993
US 5752073 A	12-05-1998	NONE	
WO 9931579 A	24-06-1999	US 6039765 A	21-03-2000
		AU 1998399 A	05-07-1999

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

1. Claims: 1-10, 15

Microprocessor executing two types of operations, fixed or user defined respectively.

2. Claims: 11-12

Central processing unit with a data stack

3. Claims: 13-14

Method for fast return from a subroutine

INTERNATIONAL SEARCH REPORT

national application No.
PCT/GB 99/03100

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-10, 15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
RL.P50896PC		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 99/03100	17/09/1999	13/10/1998
Applicant		
DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 5 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [X] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
[redacted]T/GB 99/03100

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/318

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 479 621 A (DURANTON MARC) 26 December 1995 (1995-12-26)	1,3,4,8
A	column 2, line 43 - line 46 column 4, line 10 - line 49 column 9	15

X	EP 0 279 953 A (TEXAS INSTRUMENTS INC) 31 August 1988 (1988-08-31)	1,3,4
Y	column 3, line 25 - line 27 column 3, line 43 -column 4, line 24 column 4, line 45 - line 55 column 5, line 13 - line 37 column 6, line 7 - line 16	2
A	column 7	2,15

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2000	26.04.00

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Moraiti, M

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
[redacted]/GB 99/03100

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ROGERS: "Emulation instruction" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 25, no. 11A, page 5576-5577-5577 XP002112146 ISSN: 0018-8689 the whole document	1,3,4
Y	---	2,5,6
Y	US 5 752 073 A (GRAY III DONALD M ET AL) 12 May 1998 (1998-05-12) column 14, line 18 - line 24 figure 7	2,5,6
X	---	1,3,4
	"REAL-TIME CISC ARCHTECTURE HW EMULATOR ON A RISC PROCESSOR" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 37, no. 3, page 605 XP000441601 ISSN: 0018-8689 the whole document	
P,A	---	1,3,4
	WO 99 31579 A (MOTOROLA INC) 24 June 1999 (1999-06-24) page 10, line 1 -page 11, line 10	

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
[redacted]/GB 99/03100

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5479621	A	26-12-1995	FR	2678401 A	31-12-1992
			DE	69229302 D	08-07-1999
			DE	69229302 T	02-12-1999
			EP	0520579 A	30-12-1992
			JP	5189240 A	30-07-1993
EP 0279953	A	31-08-1988	DE	3750721 D	08-12-1994
			DE	3750721 T	16-03-1995
			JP	63228225 A	22-09-1988
			US	5235686 A	10-08-1993
US 5752073	A	12-05-1998	NONE		
WO 9931579	A	24-06-1999	US	6039765 A	21-03-2000
			AU	1998399 A	05-07-1999

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB 99/03100

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-10, 15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

1. Claims: 1-10, 15

   Microprocessor executing two types of operations, fixed or user defined respectively.

2. Claims: 11-12

   Central processing unit with a data stack

3. Claims: 13-14

   Method for fast return from a subroutine

PATENT COOPERATION TREATY

OA 7/11
RL + file

From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
Lind, Robert
MARKS & CLERK
4220 Nash Court
Oxford Business Park South
Oxford 0X4 2RU
GRANDE BRETAGNE

PCT

WRITTEN OPINION

(PCT Rule 66)

Date of mailing *(day/month/year)*	07.08.2000
REPLY DUE	**within 3 month(s)** from the above date of mailing
Applicant's or agent's file reference: RL.P50896PC	
International application No.: PCT/GB99/03100	International filing date *(day/month/year)*: 17/09/1999 — Priority date *(day/month/year)*: 13/10/1998
International Patent Classification (IPC) or both national classification and IPC: G06F9/318	
Applicant: DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.	

1. This written opinion is the **first** drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

I	☒	Basis of the opinion
II	☐	Priority
III	☒	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	☐	Certain document cited
VII	☐	Certain defects in the international application
VIII	☐	Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also: For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis.
For an informal communication with the examiner, see Rule 66.6.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 13/02/2001.

Name and mailing address of the international preliminary examining authority:
European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0 Tx: 523656 epmu d
Fax: +49 89 2399 - 4465

Authorized officer / Examiner
Mengele, S

Formalities officer (incl. extension of time limits)
Schall, H
Telephone No. +49 89 2399 2647

I. Basis of the opinion

1. This opinion has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed".*):

Description, pages:

1-11 as originally filed

Claims, No.:

1-15 as originally filed

Drawings, sheets:

1/5-5/5 as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. This opinion has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been and will not be examined in respect of:

☐ the entire international application,

☒ claims Nos. 9-14,

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (*specify*):

☐ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. are so unclear that no meaningful opinion could be formed (*specify*):

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

☒ no international search report has been established for the said claims Nos. 9-14.

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-10,15
Inventive step (IS)	Claims	
Industrial applicability (IA)	Claims	

2. Citations and explanations

see separate sheet

1. **ad section IV:**

For the reasons enclosed in the invitation to pay additional fees and given under section 2.2 below, the subject-matter of Claims 1-10 and 15, the subject-matter of Claims 11-12 and the subject-matter of Claims 13-14 lack unity a posteriori.

2. **ad section V:**

2.1 Reference is made to the following document:

D1 = US-A-5,479,621.

2.2 D1 (see in particular the abstract, column 1, line 14 to column 2, line 53 with Fig. 1 and column 4, lines 11 to 48) already disclose a data processor comprising the features specified in lines 2 to 9 of Claim 1, with the claimed "fixed or predefined operation" corresponding to the "directly executable instructions" of D1, which would be executed directly in hardware (see column 1, lines 41 and 42 of D1), and the claimed "user defined operation" corresponding to the "sub-program" of D1 (see column 1, lines 42 to 45 as well as column 1, last two lines of D1).

While D1 does not explicitly mention that the disclosed data processor can be implemented as a microprocessor system, such an implementation is self-evident for the skilled person given the trend towards integrated circuit realisation of data processors.

Therefore, the subject-matter of Claim 1 does not involve an inventive step.

2.3 The feature introduced in Claim 2 is described as to be known in the prior art, see in D1 column 1, lines 40 to 51.

It is obvious for the skilled person that the addressable sub-program of D1 would be stored in a dedicated memory, e.g. a so-called "data memory" as specified in

Claim 3 of the present application.

Address generation as specified in Claim 4 is known from D1, see column 1, lines 65 to 67.

The further implementation details introduced in Claims 5 to 10 and 15 appear to lie within the normal design activity of the skilled person.

Therefore, the subject-matter of Claims 2 to 10 and 15 do not involve an inventive step.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
RL.P50896PC		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/03100	17/09/1999	13/10/1998
International Patent Classification (IPC) or national classification and IPC G06F9/318		
Applicant DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
08/05/2000	17.01.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Mengele, S Telephone No. +49 89 2399 2720

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/03100

I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-11	as originally filed				

Claims, No.:

1-15	as received on	06/11/2000	with letter of	06/11/2000	

Drawings, sheets:

1/5-5/5	as originally filed				

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-15
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-15
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

1. ad section V:

1.1 None of the documents cited in the International Search Report concerns a microprocessor system for executing Virtual Machine **bytecodes** which have been translated into respective 8 bit microprocessor instructions, wherein, in the event that an instruction corresponds to a fixed and predefined operation, the instruction is passed to the central processing unit for execution and, in the event that an instruction corresponds to a user defined operation, a subroutine corresponding to the instruction is called.

The closest prior art known from US-A-5,479,621 (D1) is particularly adapted to a FORTH type language. It anticipates the principle of having both directly executable instructions which are executed directly in hardware and indirectly executable instructions which are executed as sub-programs. However, instead of providing the means for **generating an address corresponding to the location of a subroutine**, as claimed in Claim 1, and the circuit for **loading** the remaining bits of **the bytecode shifted left by a number of bits into the microprocessor's program counter register**, as specified in Claim 15, the prior art known from D1 regards the **instructions** which it cannot execute directly **directly as addresses** of a sub-program. In order to have sufficient address-space for the sub-programs, the prior art known from D1 makes use of relatively long instructions, whereas the present invention provides 8-bit instructions in combination with address generating means, such as shifting the instruction left by a number of bits.
None of the other documents cited in the International Search Report suggests combination of 8-bit instructions with means for generating an address corresponding to the location of a subroutine.

That is, the common concept linking the subject-matter of independent Claims 1 and 15 is not rendered obvious by the available prior art.

1.2 Dependent Claims 2 to 14 specify embodiments of the subject-matter of Claim 1.

2. ad section VII:

2.1 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document D1 is not mentioned in the description, nor is this document identified therein.

2.2 Description pages 3 to 6 are not in conformity with the claimed subject-matter.

CLAIMS

1. A microprocessor system for executing Virtual Machine bytecodes which have been translated into respective 8-bit microprocessor instructions which correspond either to a fixed and predefined operation or to a user defined operation, the system comprising:

a central processing unit;

an instruction memory for storing the sequence of 8-bit microprocessor instructions;

means for fetching each stored instruction in turn and for analysing each instruction to determine whether an instruction corresponds either to a fixed and predefined operation or to a user defined operation;

means for generating an address corresponding to the location of a subroutine if an instruction corresponds to a user defined operation,

wherein, in the event that an instruction corresponds to a fixed and predefined operation, the instruction is passed to the central processing unit for execution and, in the event that an instruction corresponds to a user defined operation, a subroutine corresponding to the instruction is called using the generated address.

2. A microprocessor system according to claim 1, wherein instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code, and the means for analysing each stored instruction is arranged to check for the presence of a bit in that bit position.

3. A microprocessor system according to claim 1 or 2, wherein the microprocessor system comprises a data memory arranged in use to store code defining said subroutines.

4. A microprocessor system according to claim 2 or to claim 3 when appended to claim 2, wherein said distinguishing bit is the most significant bit of the instruction code, and the generating means is arranged to shift the code to the left by one or more bits.

5. A microprocessor system according to claim 4 and comprising a program counter register which is arranged to load the bit shifted instruction.

6. A microprocessor system according to claim 3, wherein the instruction memory is arranged to hold 8-bit wide instructions, whilst the data memory is arranged to hold 32-bit data values.

7. A microprocessor system according to any one of the preceding claims and comprising a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory when execution of the subroutine is completed.

8. A microprocessor system according to claim 7, wherein the central processing unit, instruction memory, data memory, hardware stack, and program counter are all coupled to a common bus.

9. A microprocessor system according to claim 8, wherein the central processing unit, instruction memory, data memory, hardware stack, program counter, and common bus are integrated onto a single chip.

10. A microprocessor system according to any one of the preceding claims, wherein the central processing unit contains an arithmetic logic unit and a data stack, and the top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

11. A microprocessor system according to claim 10, wherein the top three elements of the data stack contain special-purpose circuits, which enable the execution of seven primitive stack operations directly in hardware.

12. A microprocessor system according to any one of the preceding claims and comprising means for recognising a "fast return" instruction "folded" with a regular instruction, by utilising circuitry which decodes the "fast call" bit in an 8-bit bytecode and another dedicated bit or bits in the 8-bit bytecode.

13. A microprocessor system according to claim 12, wherein said other dedicated bit is the second most significant bit in the 8-bit bytecode.

14. A microprocessor system according to any one of the preceding claims, wherein said Virtual Machine bytecodes are Java bytecodes.

15. A microprocessor system, consisting of a central processing unit, 8-bit wide instruction memory, 32-bit wide data memory and a hardware stack connected via an internal bus to the program counter register, together with an instruction decode unit which includes a circuit for detecting the presence of a distinguished bit in the 8-bit bytecode, together with a circuit for loading the remaining bits of the bytecode shifted left by a number of bits into the microprocessor's program counter register, while at the same time storing the current value of the program counter register on the aforementioned stack.

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

Lind, Robert
MARKS & CLERK
4220 Nash Court
Oxford Business Park South
Oxford 0X4 2RU
GRANDE BRETAGNE

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	17.01.2001
Applicant's or agent's file reference RL.P50896PC	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/03100	17/09/1999	13/10/1998

Applicant
DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

   The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

   Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

   For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Schall, H Tel.+49 89 2399-2647

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
RL.P50896PC		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/03100	17/09/1999	13/10/1998
International Patent Classification (IPC) or national classification and IPC G06F9/318		
Applicant DIGITAL COMMUNICATION TECHNOLOGIES LTD et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
08/05/2000	17.01.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Mengele, S Telephone No. +49 89 2399 2720

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/03100

I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-11	as originally filed				

Claims, No.:

1-15	as received on	06/11/2000	with letter of	06/11/2000	

Drawings, sheets:

1/5-5/5	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-15
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-15
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

1. **ad section V:**

1.1 None of the documents cited in the International Search Report concerns a microprocessor system for executing Virtual Machine **bytecodes** which have been translated into respective 8 bit microprocessor instructions, wherein, in the event that an instruction corresponds to a fixed and predefined operation, the instruction is passed to the central processing unit for execution and, in the event that an instruction corresponds to a user defined operation, a subroutine corresponding to the instruction is called.

The closest prior art known from US-A-5,479,621 (D1) is particularly adapted to a FORTH type language. It anticipates the principle of having both directly executable instructions which are executed directly in hardware and indirectly executable instructions which are executed as sub-programs. However, instead of providing the means for **generating an address corresponding to the location of a subroutine**, as claimed in Claim 1, and the circuit for **loading** the remaining bits of **the bytecode shifted left by a number of bits into the microprocessor's program counter register**, as specified in Claim 15, the prior art known from D1 regards the **instructions** which it cannot execute directly **directly as addresses** of a sub-program. In order to have sufficient address-space for the sub-programs, the prior art known from D1 makes use of relatively long instructions, whereas the present invention provides 8-bit instructions in combination with address generating means, such as shifting the instruction left by a number of bits.
None of the other documents cited in the International Search Report suggests combination of 8-bit instructions with means for generating an address corresponding to the location of a subroutine.

That is, the common concept linking the subject-matter of independent Claims 1 and 15 is not rendered obvious by the available prior art.

1.2 Dependent Claims 2 to 14 specify embodiments of the subject-matter of Claim 1.

2. ad section VII:

2.1 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document D1 is not mentioned in the description, nor is this document identified therein.

2.2 Description pages 3 to 6 are not in conformity with the claimed subject-matter.

MARKS & CLERK
Intellectual Property

European Patent Attorneys
Chartered Patent Attorneys
European Trade Mark Attorneys
Registered Trade Mark Attorneys

Established 1887

Oxford Office
4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU

Tel: +44 (0)1865 397900
Fax: +44 (0)1865 397919
E-mail: oxadmin@marks-clerk.com
http://www.marks-clerk.com

The European Patent Office
EPA/EPO/OEB
D-80298 Munchen
Germany

your ref

our ref RL.P50896PC

date 6 November 2000

By fax & mail
(7 pages)

Dear Sirs,

PCT Application No. PCT/GB99/03100
Filed 17 September 1999 claiming priority from
GB Patent Application No. 9822191.4 filed 13 October 1998
Digital Communication Technologies Ltd

In response to your communication dated 7 August 2000 we enclose herewith in triplicate a replacement set of claims pages 12 to 14. Claim 1 has been amended to relate to a microprocessor system for executing Virtual Machine bytecodes (page 2, 3rd paragraph). Claim 1 now additionally states that the system has "means for generating an address corresponding to the location of a subroutine if an instruction corresponds to a user defined operation". This means may be the Address Generator circuit referred to at page 7, lines 9 and 10. Original claim 3 has been deleted and claims 4 to 14 renumbered 3 to 13 respectively. A new claim 14 has been added, whilst original claim 15 remains unchanged.

Java is designed to run on a so-called Java Virtual Machine (JVM). The JVM defines an 8-bit instruction set - each instruction is called a "bytecode". In practice, JVMs are emulated using processors such as Pentium™ processors. This requires a translation to be made between the 8 bit Java instructions and the 32 bit instructions used by Pentium processors.

The starting point for this invention is a desire to provide a low cost, but still efficient, Java based microprocessor. This means that the memory requirements must be low, and the architecture simple. In order to satisfy the first requirement, we want the executable code to be small, using only 8 bit wide instructions. In the past, it has been proposed to achieve this by designing a microprocessor which directly executes Java bytecode, i.e. the microprocessor has a physical structure and mode of operation corresponding to a JVM.

However, many of the JVM instructions are very costly to implement in hardware. This

means that such a Java processor must either be complex (costly) or it must implement some of the complicated JVM instructions via a subroutine mechanism (which carries a speed penalty).

In order to reduce the overheads of implementing JVM instructions, the inventors of the present invention have recognised that it is advantageous to transform the Java bytecodes into 8 bit instructions which have a structure which allows directly executable (simple) instructions to be easily distinguishable from instructions which are implemented by a subroutine call (the translation between the Java bytecodes and the 8 bit instructions is easily achieved using for example a one-to-one mapping mechanism). Whilst the translation step itself involves some processing overheads, this is more than compensated for by the fast subroutine call mechanism which translation facilitates. It is the operation on **translated** 8 bit instructions which provides the inventive step over the known architectures for executing Java. This is not taught in any of the documents cited in the International search report.

It is not the case that designing a microprocessor which operates on a transformed instruction set is an obvious step to take in view of US5,479,621 (Philips). In that patent, instructions which require a subroutine call contain the address where the subroutine can be found. Subroutines necessarily contain multiple instructions located in sequential memory locations. For example, if we have 50 subroutines each taking 8 memory locations, the subroutines will occupy a block of 400 memory locations. The microprocessor of the Philips patent makes use of relatively long instructions, i.e. 16 and 32 bits. These instructions are used to directly encode subroutine locations and are more than long enough for that purpose, even after an identifying bit has been stripped off.

As has already been noted, the present invention uses 8 bit executable instructions. An 8 bit instruction can only identify 128 consecutive memory locations (since one bit is used to tag the instruction as a subroutine call) which is wholly insufficient to support the required number of subroutines. In the light of the Philips patent, the skilled person would conclude that it is not possible to implement a microprocessor which operates on 8 bit instructions generated by translating Java bytecode, and would either return to the costly (or slow) JVM type architecture or to the expensive (in terms of memory usage) architecture using 32-bit (or wider) instructions. The Philips patent does not enable the skilled man to make a microprocessor which can execute 8 bit instructions.

Contrary to what the skilled man would have concluded from the Phillips patent, it has now been recognised that the problem of limited address range in an 8 bit instruction can be overcome by generating a subroutine address using the instruction as a basis. More particularly, this generating step involves an expansion of the instruction (or rather a part of the instruction). In the specific example described in the application, an instruction requiring a subroutine call is shifted to the left by two bits. The expanded instruction provides access to a 512 byte memory block and allows the addressing of 128 distinct memory locations each

separated by 4 bytes. However, other mechanisms for expanding the subroutine address encoded in an 8-bit instruction are conceivable.

It is submitted that in the light of the amendments made to the claims the Office should now issue a favourable opinion in respect of claim 1. In the event that the examiner has any remaining concerns, the undersigned would appreciate the opportunity to discuss the case with him on the telephone.

Please acknowledge receipt of this letter by returning the enclosed form EPO 1037.

Yours faithfully,
for Marks & Clerk

Dr. Robert Lind

Enc.

CLAIMS

1. A microprocessor system comprising:

a central processing unit;

an instruction memory for storing a sequence of instructions which correspond either to a fixed and predefined operation or to a user defined operation; and

means for fetching each stored instrucion in turn and for analysing each instruction to determine whether an instruction corresponds either to a fixed and predefined operation or to a user defined operation and, in the former case, for passing the instruction to the central processing unit for execution or, in the latter case, for calling a subroutine corresponding to the instruction.

2. A microprocessor system according to claim 1, wherein instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code, and the means for analysing each stored instruction is arranged to check for the presence of a bit in that bit position.

3. A microprocessor system according to claim 1 or 2, wherein the microprocessor system comprises a data memory arranged in use to store code defining said subroutines.

4. A microprocessor system according to claim 3, wherein the system comprises means for generating an address corresponding to the location of a subroutine if an instruction corresponds to a user defined operations.

5. A microprocessor system according to claim 4, wherein said distinguishing bit is the most significant bit of the instruction code, and the generating means is arranged to shift the code to the left by one or more bits.

6. A microprocessor system according to claim 5 and comprising a program counter register which is arranged to load the bit shifted instruction.

7. A microprocessor system according to any one of claims 3 to 6, wherein the instruction memory is arranged to hold 8-bit wide instructions, whilst the data memory is arranged to hold 32-bit data values.

8. A microprocessor system according to any one of the preceding claims and comprising a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory when execution of the subroutine is completed.

9. A microprocessor system according to claim 8, wherein the central processing unit, instruction memory, data memory, hardware stack, and program counter are all coupled to a common bus.

10. A microprocessor system according to claim 9, wherein the central processing unit, instruction memory, data memory, hardware stack, program counter, and common bus are integrated onto a single chip.

11. A microprocessor system according to any one of the preceding claims, wherein the central processing unit contains an arithmetic logic unit and a data stack, and the top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

12. A microprocessor system according to claim 11, wherein the top three elements of the data stack contain special-purpose circuits, which enable the execution of seven primitive stack operations directly in hardware.

13. A microprocessor system according to any one of the preceding claims and comprising means for recognising a "fast return" instruction "folded" with a regular instruction, by utilising circuitry which decodes the "fast call" bit in an 8-bit bytecode and another dedicated bit or bits in the 8-bit bytecode.

14. A microprocessor system according to claim 13, wherein said other dedicated bit is the second most significant bit in the 8-bit bytecode.

15. A microprocessor system, consisting of a central processing unit, 8-bit wide instruction memory, 32-bit wide data memory and a hardware stack connected via an internal bus to the program counter register, together with an instruction decode unit which includes a circuit for detecting the presence of a distinguished bit in the 8-bit bytecode, together with a circuit for loading the remaining bits of the bytecode shifted left by a number of bits into the microprocessor's program counter register, while at the same time storing the current value of the program counter register on the aforementioned stack.